

WHAT IS CLAIMED IS:

1. A serial interface for use in a programmable logic device, said serial interface comprising:
 - a plurality of channels, each of said
 - 5 channels including at least transmit circuitry;
central control circuitry including at least one clock source for generating at least one transmit clock for use by said transmit circuitry in each of said channels, each said transmit clock having a
 - 10 respective first clock rate; and
clock division circuitry in at least one of said channels for providing from at least one said transmit clock a channel-derived clock having a second clock rate at most equal to said respective first clock
 - 15 rate.
2. The serial interface of claim 1 wherein each of said channels includes said clock division circuitry.
3. The serial interface of claim 1 wherein said clock division circuitry comprises a respective first divider that selectably divides said respective first clock rate by one of a group of at least one integer
- 5 value.
4. The serial interface of claim 3 wherein said one of said group of at least one integer value is selected by user programming of said programmable logic device.
5. The serial interface of claim 3 wherein said one of said group of at least one integer value is selected under control of logic in said programmable logic device.

6. The serial interface of claim 3 wherein said group of at least one integer value consists of one integer value.

7. The serial interface of claim 3 wherein said group of at least one integer value comprises a plurality of integer values.

8. The serial interface of claim 1 further comprising a selector for selecting as said channel-derived clock one of (a) one said least one transmit clock, and (b) output of said clock division circuitry.

9. The serial interface of claim 8 wherein said selector comprises a multiplexer.

10. The serial interface of claim 1 wherein said at least one clock source consists of a single clock source generating a single transmit clock having a single transmit clock rate.

11. The serial interface of claim 1 wherein said at least one clock source comprises a plurality of clock sources, each of said clock sources generating its own respective first clock rate.

12. The serial interface of claim 11 further comprising a selector for selecting as said channel-derived clock one of (a) one of said plurality of clock sources, and (b) output of said clock division circuitry.

13. The serial interface of claim 12 wherein said selector comprises a multiplexer.

14. The serial interface of claim 11 wherein:
said clock division circuitry comprises a respective divider for dividing each said respective first clock rate by a respective selectable integer value; and

5 said serial interface further comprises a selector for selecting said channel-derived clock from among outputs of said respective dividers.

15. The serial interface of claim 14 wherein said selector comprises a multiplexer.

16. The serial interface of claim 1 wherein:
each said transmit clock is a serial clock
5 and each said respective first clock rate is a serial clock rate;

 said central control circuitry further comprises, for each said at least one clock source, a divider for deriving from each said transmit clock a
10 respective parallel clock having a respective parallel clock rate; and

 said clock division circuitry derives a channel-derived serial clock having a second clock rate at most equal to said respective first clock rate, and a
15 channel-derived parallel clock having a channel-derived parallel clock rate at most equal to said respective parallel clock rate.

17. A programmable logic device comprising the serial interface of claim 1.

18. A digital processing system comprising:
processing circuitry;
a memory coupled to said processing
circuitry; and
5 a programmable logic device as defined in claim 17 coupled to the processing circuitry and the memory.

19. A printed circuit board on which is mounted a programmable logic device as defined in claim 17.

20. The printed circuit board defined in claim 19 further comprising:

memory circuitry mounted on the printed
circuit board and coupled to the programmable logic
5 device.

21. The printed circuit board defined in claim
20 further comprising:

processing circuitry mounted on the printed
circuit board and coupled to the memory circuitry.

22. An integrated circuit device comprising the
serial interface of claim 1.

23. A digital processing system comprising:
processing circuitry;

a memory coupled to said processing
circuitry; and

5 an integrated circuit device as defined in
claim 22 coupled to the processing circuitry and the
memory.

24. A printed circuit board on which is mounted
an integrated circuit device as defined in claim 22.

25. The printed circuit board defined in claim
24 further comprising:

memory circuitry mounted on the printed
circuit board and coupled to the integrated circuit

5 device.

26. The printed circuit board defined in claim
25 further comprising:

processing circuitry mounted on the printed
circuit board and coupled to the memory circuitry.

27. A programmable logic device comprising:

a programmable logic core; and

serial interface means comprising:

a plurality of channel means, each of said

5 channel means including at least transmit means;

central control means including at least one clock means for generating at least one transmit clock for use by said transmit means in each of said channel means, each said transmit clock having a respective first
10 clock rate; and

clock division means in at least one of said channel means for providing from at least one said transmit clock a channel-derived clock having a second clock rate at most equal to said respective first clock
15 rate.